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Quarterly Technical Progress Report of the Information Engineering Laboratory for the period August-October 1977

November 1977

DEPARTMENT OF COMPUTER SCIENCE
UNIVERSITY OF ILLINOIS AT URBANA-CHAMPAIGN · URBANA, ILLINOIS

Quarterly Technical Progress Report
of the
Information Engineering Laboratory
for the period
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Department of Computer Science
University of Illinois at Urbana-Champaign
Urbana, Illinois 61801

1. Introduction

This report is intended to keep interested persons informed about the progress on various research projects being carried out by the Information Engineering Laboratory of the Department of Computer Science. Each report lists those projects which have been completed, summarizes progress on those which are currently active, and provides introductory remarks on new projects.

Through September of this quarter, the primary source of funding for these projects was through the Office of Naval Research on Contract N00014-75-C-0982. This report includes both ONR funded research and research funded by other (or no) agencies. Each section of the report is divided into a part pertaining to ONR funded research and a part pertaining to research supported by other funds. In the latter case, the source is specified.

The research is carried out by half-time graduate research assistants (graduate students) under the direction of one or more faculty members. The final documentation on a given project is usually in the form of the students thesis (MS or Ph.D.). These theses are published as technical reports on the projects and are listed, along with an abstract in the "projects completed" section of this report. In some cases technical reports are issued which are not theses and these are also listed.

Some of the research is the result of a research proposal and in such cases a more detailed account of the proposed research can be found by consulting the relevant proposal. In other cases the research is a result of ideas originating with a student or staff member. In either case, an introductory description of the proposed research appears when a new project is introduced into the report. Thereafter only a brief synopsis is included.

Section two summarizes the projects completed during the quarter, section three presents progress reports on current projects, and section four introduces new projects. Projects are listed by name and a corresponding project number is given in parentheses.

2. Summary of Projects Completed During the Quarter

The projects completed this quarter are listed below by project name and number along with the technical report number and the abstract. Some reports are available directly from the Department of Computer Science, University of Illinois, Urbana, IL 61801. Others may be obtained from the Engineering Documents Center, 208 Engineering Hall, University of Illinois, Urbana, IL 61801 or from the IEEE Computer Society Repository, 5855 Naples Plaza, Suite 301, Long Beach, CA 90803.

2.1 ONR Funded Projects

WALSHSTORE (#78)

"WALSHSTORE: THE APPLICATION OF BURST PROCESSING TO FAIL-SOFT STORAGE SYSTEMS USING WALSH TRANSFORMS", Bracha, Ehud, Report #UIUCDCS-R-77-878.

ABSTRACT

WALSHSTORE is concerned with the investigation into the application of orthogonal transforms, e.g., Walsh transforms, to the storage of visual images in a fail-soft manner, i.e., the system can sustain losses but the retrieved image can still be recognized, even if in a degraded form.

The application of Burst Processing to various parts in such a system is investigated together with an analysis of the amount of storage and speed of computation that can be achieved.

This paper presents the necessary theory and the implementation of the Walsh transformers and the fail-soft storage which were constructed and tested. Additionally, some software simulation results are compared to the actual machine performance.

2.2 Non-ONR Funded Projects

Source of funding is given in brackets: [source].

None this quarter.

3. Progress Report on Continuing Projects

3.1 ONR Funded Projects

PREDICTORBURST (#81)

INTRODUCTION

The goal of this project is the real-time extraction of predictor coefficients from a human voice signal. These coefficients, used in the linear prediction of speech, are employed so as to encrypt the message or transmit it over narrow band digital data lines. The previous quarterly report showed the general system topology for the adaptive filter which generates the coefficients.

PROJECT STATUS

A full feedback loop has been completed for one stage of the filter, corresponding to a predictor of order one, thus estabilishing signal compatibility among the various components. Determination of the effectiveness of the prediction cannot be done at this point, except that examination of the residual signal on an oscilloscope shows a reduction in magnitude on the order of 50%. To better analyze the internal operation of the circuit, a necessity for determining the final topology, simulation of the device is required and will occupy the bulk of the research effort for the next quarter.

Daniel A. Pitt

INDIRAD (#82)

INTRODUCTION

INDIRAD is a digital AM receiver which uses indicator representation for high speed processing.

PROJECT STATUS

During the last quarter, computer simulations of the radio have been run and the design parameters set. Construction of the hardware will begin when parts are received.

As shown in Fig. 3.1 the circuits to extract the SINE and COSINE of the desired signal are identical low pass filters. Each must cycle at F_c, the frequency of the carrier, but SIN CK preceedes COS CK by $\frac{1}{4F_c}$. Since each circuit must cycle in 10 nsec. to receive a 100 MHz station, only the simplest filtering methods could be considered. A decision was made to use a Finite Impulse Response filter having a rectangular window (Fig. 3.2a) for 50-100 MHz and a "bi-rectangular" window (Fig. 3.2b) for 0-50 MHz. These windows have stopbands 13.25 db down and 19.16 db down, respectively from the passband. The bi-rectangular window can easily be obtained by double clocking the summation block register and counter. This avoids any multiplications which are usually slow. The output sample rate of the filter is much slower than the input rate due to the decimation of the filter.

The RF waveform will be encoded into 7 levels. Each sequence of samples will be low pass filtered by a summation block and a 12 bit counter. The 4 most significant bits of the result will be selected from the counter by the 4x4 multiplexer and used to determine the carrier amplitude. Any overflow of the counters or the analog-to-count converter severely degrades performance of the radio. A typical signal to noise ratio of 22 db is expected.

Gary Gostin

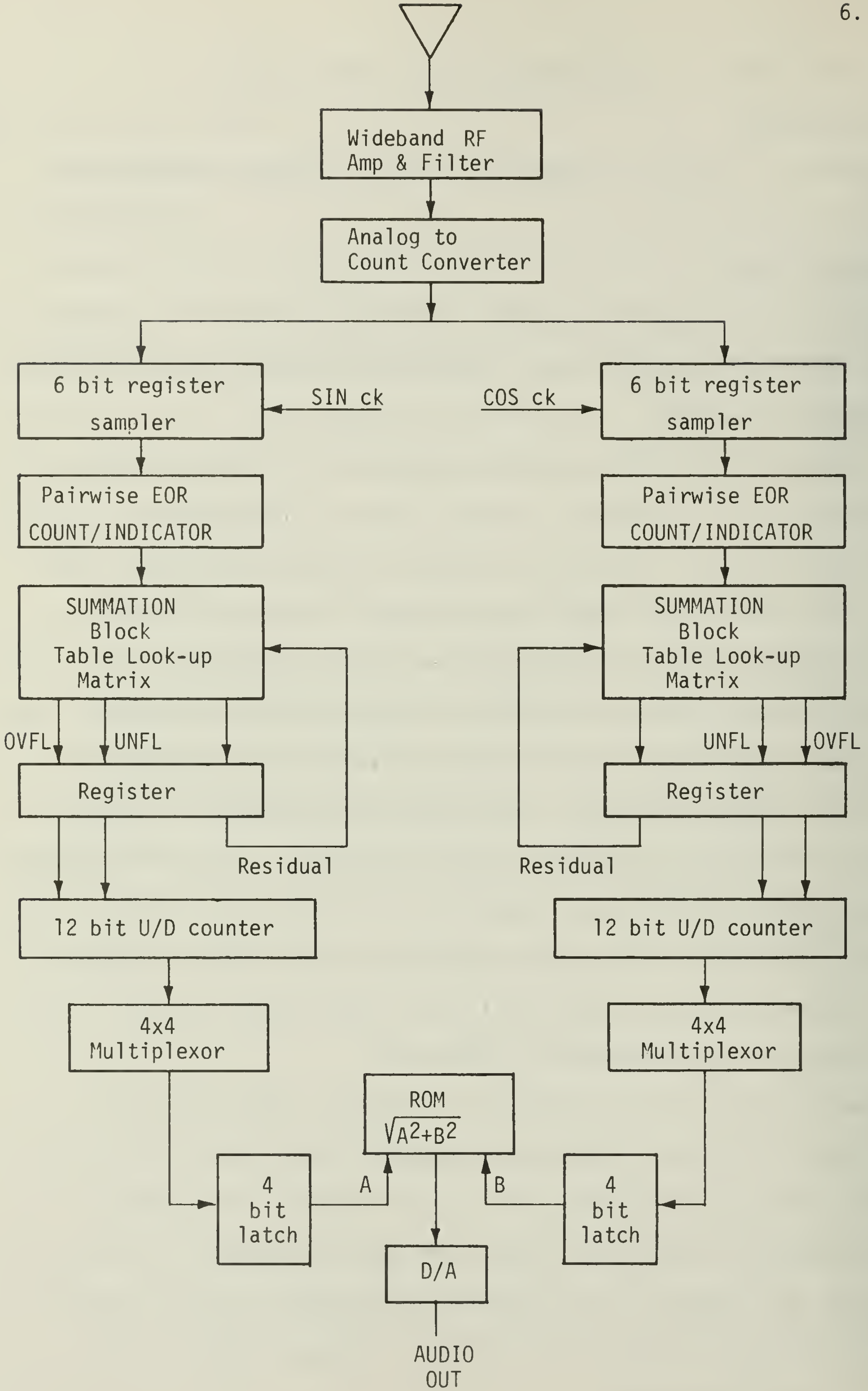

Figure 3.1 Block Diagram of INDIRAD

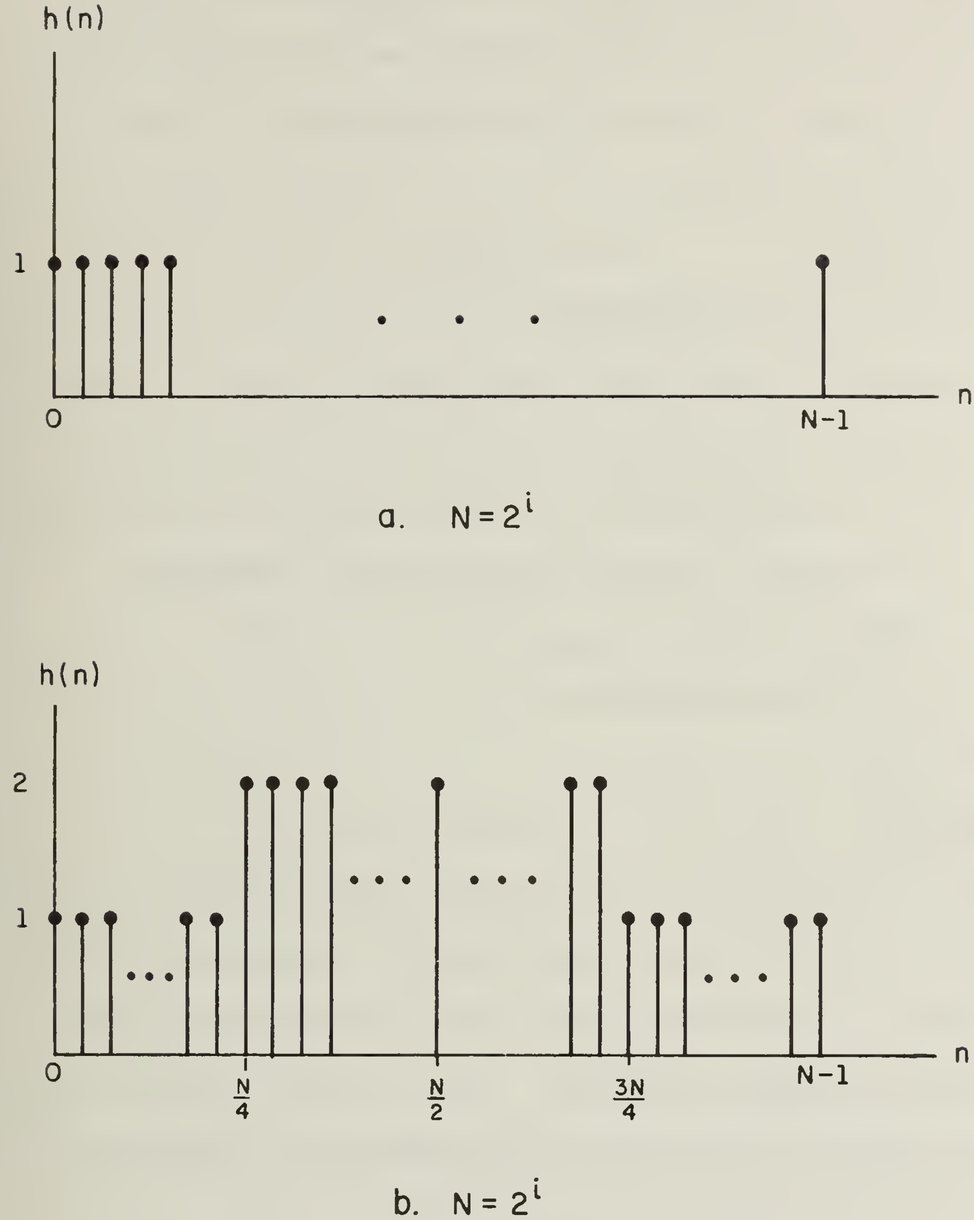

Figure 3.2 FIR Filter Responses for INDIRAD

NETSURV (#84)

INTRODUCTION

This project is concerned with the design of a communication network of limited extent (a ship or building) which has properties such that its expected survivability is high even when it suffers multiple communication path loss.

PROJECT STATUS

This project has been terminated.

BURFT II (#85)

INTRODUCTION

This project is an extension of the BURFT project with the goal of implementing more general transforms than the Fourier Transform.

PROJECT STATUS

This project has been terminated.

ILLIBOT (#86)

INTRODUCTION

The goal of this project is to construct a robot capable of surviving totally on its own in a potentially hostile environment. The robot will require no human guidance or interference under normal operating conditions.

REVIEW OF THE CONCEPT OF ILLIBOT:

Illibot's purpose is to survive, obey commands and construct an understanding of the world.

Illibot normally operates through its primary control system which assigns service priorities to occurences in the enivronment as follows:

Highest	1.	Reversal of harm to humans and materials
	2.	Surviving
	3.	Listening
	4.	Sight Control
	5.	Speaking
	6.	Moving
Lowest	7.	Environmental Changes

However, upon indication of low batteries, Illibot initializes its secondary control system thus entering the SURVIVE mode. This mode, facilitating rapid movement to an outlet, reorders the service priorities as follows:

New level	Old level	
1.	1.	Reversal of harm to humans and materials
2.	2.	Surviving
3.	6.	Moving
4.	7.	Environmental Changes
5.	4.	Sight Control
6.	5.	Speaking
7.	3.	Listening

PHYSICAL CONFIGURATION OF ILLIBOT:

During the last quarter, the physical configuration of past robots has been studied in order to optimize that of Illibot.

After considering the goal of Illibot's operation and its operating environment, the following physical implementations are proposed. (See Figure 3.3).

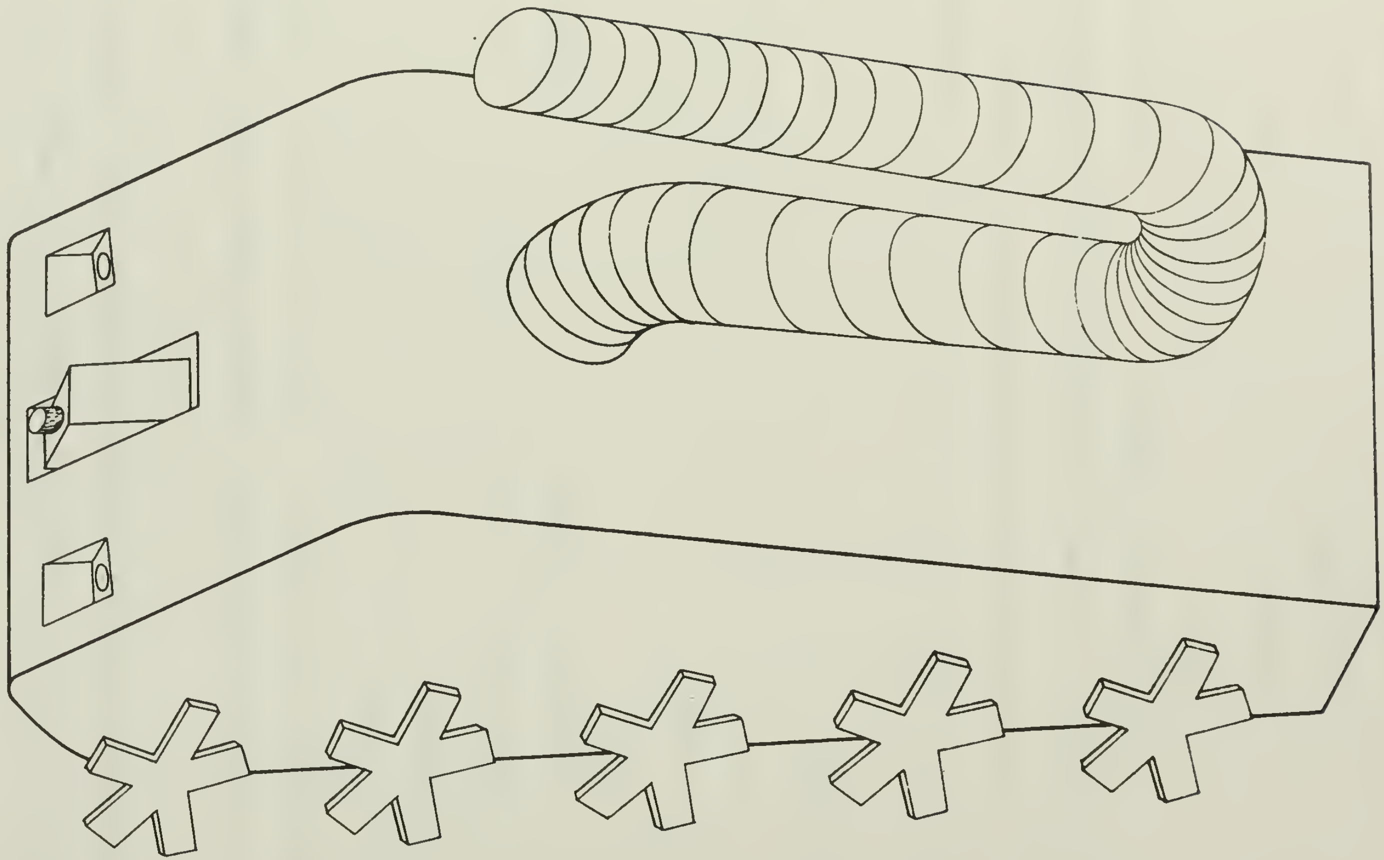

Figure 3.3 Physical Configuration of ILLIBOT

The low profile 'tank' design is proposed in order to maintain high stability while moving along a grade. The centered, multi-jointed arm aids in maintaining a low center of gravity in addition to being positioned in an optimal location for manipulative tasks. The most obvious 'oddity' in the drawing is the shape of the wheels. There are five equiangular pentagonal 'wheels' on each side of the robot. The reasoning behind these stems from the goal of the project; '... to construct a robot capable of surviving totally on its own in a potentially hostile environment.' Though one might not consider a staircase or other physical obstruction hostile, it is a problem that is difficult to deal with in contemporary robotics. These special wheels have proved to be the optimum arrangement for locomotion, since square wheels will get stuck on stairs, whereas hexagonal wheels will slip. In addition to their unusual shape, each wheel is offset 14.4 degrees from the next. Thus, while moving on a flat surface, at least 6 of the 10 wheels will be on the ground and, on a staircase, at least 8 of 10 wheels will touch.

The camera (only one is shown in the figure but a second is being considered for stereo viewing) is mounted on a 3-axis gimbal under full control of the picture processing subsystem. This special mount is used so that the machine can observe, and thus direct visually, any manipulation required of the arm.

Another obvious object missing from Figure 3.3 is the hand. It is shown in Figure 3.4. Its design is adapted to the manipulation of objects encountered in everyday life; it is modelled after the human hand.* Two of the three fingers operate in unison while the third operates independently, emulating a 'thumb'.

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*Minsky, Marvin, MANIPULATOR DESIGN VIGNETTES Artificial Intelligence Memo No. 267, Massachusetts Institue of Technology, Artificial Intelligence Laboratory, October, 1972.

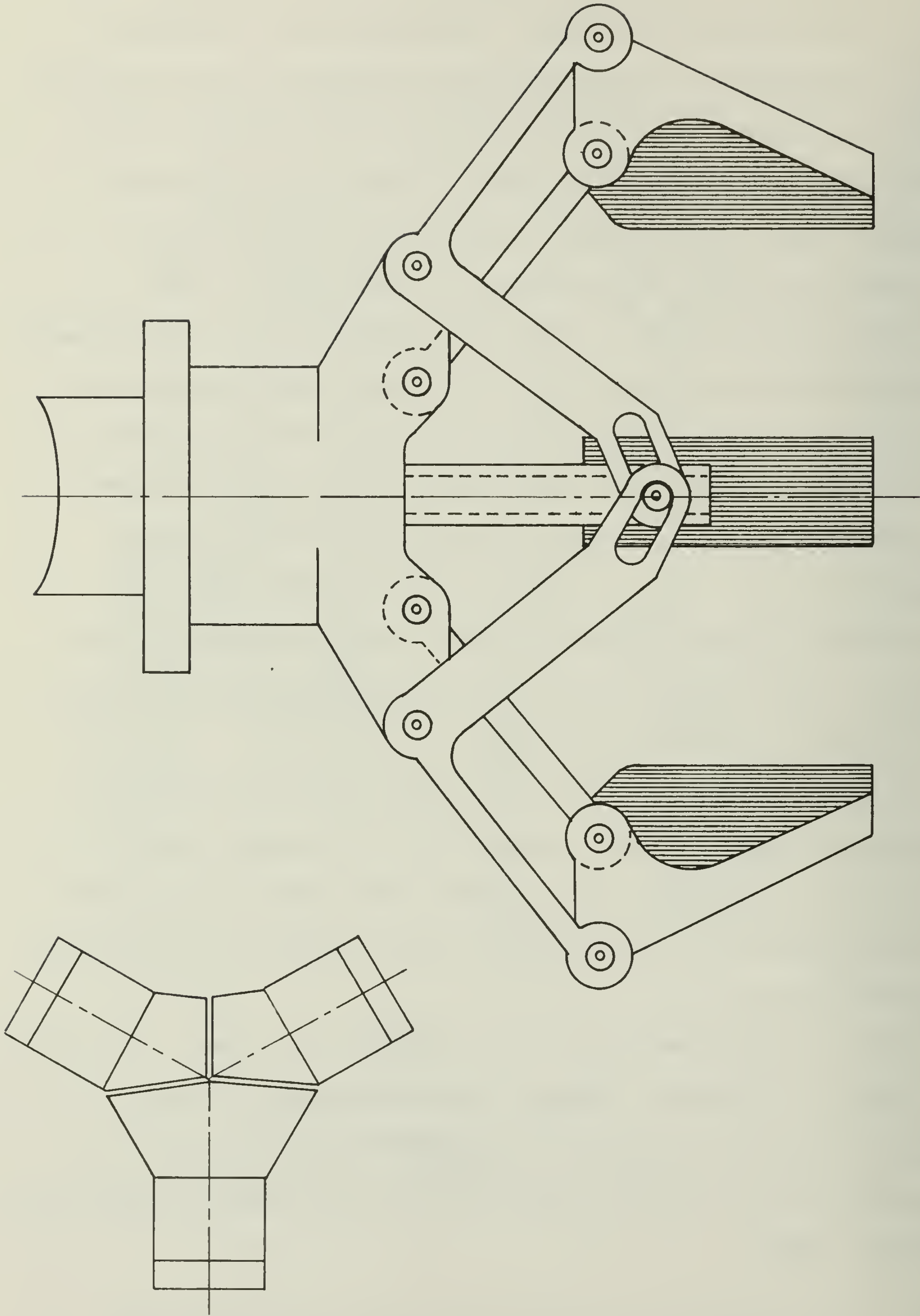

Figure 3.4 ILLIBOT Hand

PROJECT STATUS

Motor timing circuits, control circuits, feedback circuits and sequencers have been tested aboard a small scale robot designated ALPHA. Practical methods of organizing Illibot so that it may successfully and efficiently deal with its environment have been developed.

Jeff Glickman

XENOCOMM (#87)

INTRODUCTION

The XENOCOMM project is an attempt to develop a system making possible communication to submarines while the submarines are submerged to depths of up to 1000 feet.

PROJECT STATUS

As noted in the last report, a high intensity pulsed light source with a repetition rate of about 10,000 pulses per second is needed for XENOCOMM. The initial idea was to use a Xenon flash lamp but it was determined that, although Xenon lamps capable of such a high repetition rate can be obtained, they are not available as stock items. Lamps designed for high repetition rates are available as a custom-designed products from at least two manufacturers and cost between $5000 and $8000.

One high intensity, high repetition rate, pulsed light source would be needed for each buoy, unless some sort of inexpensive "light valve" could be developed. That is, if a single light source is mounted on the submarine, the buoy would require only a device that would either reflect or not reflect some of the light back to the submarine depending on the signal being received by the radio in the buoy. The light valve

would have to operate at a repetition rate of at least 10,000 pulses per second, as was the case with the lamp. With either approach XENOCOMM boys would be expensive.

At this point in the project the funding was discontinued and no further work is planned.

Randy Moss

PLANOBURST (#88)

INTRODUCTION

PLANOBURST uses Burst unary processors to implement a class of matrix processing functions characterized by two main features: First the operation performed on a particular element is solely a function of the elements in a small surrounding neighborhood, and second, the operation is to be repeated a number of times.

PROJECT STATUS

The previous quarterly report detailed the general concept of PLANOBURST as a matrix processor for a class of matrix operations characterized by the fact that the processing of an element was dependent on only a small surrounding neighborhood. It was pointed out that there is a wide range of applications for this technique, but that the actual design depends largely on the scope of the problems to be undertaken. In particular, it is clear that it would be unwise to attempt to implement the most general version of the processor since the desirable form in which to output the resultant matrix varies so widely from problem to problem.

Therefore, the past quarter has been devoted mainly to selecting and defining the area of application. It was decided that the processor should form the front end of an image recognition and classification

scheme which would operate in real time, performing preliminary enhancement and error correction on a binary video input. The real time requirement precluded the use of the interative feature described in the previous report, except that it is possible to cascade identical processors in order to provide a fixed number of iterations.

The processor looks at the matrix through an nxn window, where n is odd, and decides what action to perform on the central element according to the other elements in the window. Clearly, even for n = 3 or 5 it is not desirable to synthesize a Boolean function of the window elements due to the large number of minterms involved. Instead, the symmetry of the function is exploited by selecting a small number of masks and attempting to match the window to them in 8 different orientations corresponding to successive 45° rotations of the masks.

Currently computer simulations are being performed to determine the content of the masks and the minimumally sufficient value of n and to investigate how the cascading of simpler processors compares to the performance of a single more complex processor.

Michael Robinson

3.2 Non-ONR Funded Projects

Source of funding is given in brackets: [Source]

Parallel Hardware Algorithms for High-Speed Function Generation (#73) [DCS]

INTRODUCTION

This project considers the problem of high speed parallel hardware function generation. The function f(x) is to be evaluated in the interval [a,b]. The interval [a,b] is broken down into a few subintervals

$[x_k, x_{k+1}]$ within which f is piecewise approximated by a polynomial. Each interval uses a different degree polynomial. x_k is called a joint. The coefficients of these poynomials are stored in ROMs. The argument x is logrithmically distributed since it is assumed to be a floating point mautissa in the interval [.5,1]. The goal is to minimize the <u>average</u> number of multiplications M(X) needed to evaluate f(x) subject to a constraint on the number of ROM words $R_0(X)$ where X is the vector of subinterval breakpoints $(x_0, x_1, \ldots x_m)$.

PROJECT STATUS

The stated goal leads to a nonlinear programming problem. There is no reliable software available affording a solution to the general problem but the method of penalty functions can be used to solve the simpler problem:

Find the minimum of: $M(.5,1) + \mu_n P(N, Ro), \mu_n \to \infty$ (1)

where N is the number of ROM words required, R_0 the limit on ROM words, P a function of N and R_0 which is null when $N \leq R_0$ and positive when $N > R_0$. The μ_n constants go to infinity and, in the limit, the minimum of (1) is a solution of the NLP.

A FORTRAN program has been written to solve the above problem for up to 3 intervals (2 joints) for the function $\frac{1}{x}$. Polynomials of degrees 1 thru 5 have been used and a set of curves showing the average number of multiplications versus the total number of stored coefficients has been obtained.

Gilles Gracia

PEARL (#83) [UIUC Research Board]

INTRODUCTION

PEARL (Portable Evoked Average Response Laboratory) is a portable, intelligent device for monitoring psychophysiological experiments and collecting data.

PROJECT STATUS

Hardware construction was completed during the summer of 1977. During the last quarter, software was written to test the system.

A complete detailed description of the hardware is to be found in the author's forthcoming Master's thesis. It includes a brief description of the experiments concerned, the hardware and software requirements of PEARL, the choice of hardware and a detailed explanation of the design. Part 3 of the thesis serves as a hardware maintenance manual which contains all necessary circuit and timing diagrams for the purposes of maintenance and troubleshooting.

To exercise all parts of the system, a program was written to monitor a typical "ODD BALL" experiment. 3 analog channels were multiplexed and digitized at 100 Hz/channel. The sampling window was 1.28 sec. wide with a 1.67 sec. inter-stimulus-interval. Processing involves calculating mean and variance, and storing data onto a digital cassette. The program has been loaded from the cassette and run successfully.

The system is packaged into a 2'x4'x1' box, weighing 26 lb. (without the power supplies), and is ready for testing application software.

Tony Mui

MICROCARDALERT (Project #94) [EE and School of Clinical Medicine]

INTRODUCTION

"CARDALERT" is a microprocessor-based cardiac signal analyzer. It detects the presence of premature ventricular contractions in heart beats due to heart diseases. By detecting these abnormal contractions, cardiac arrests can be predicted.

PROJECT STATUS

The building, testing, and debugging of the circuitry utilized with the microprocessor and its related components is in the final stages. In addition, the data sampling circuitry and the control panel are almost complete. The process of integrating the various parts of the microprocessor - based cardiac signal analyzer system to assure viability has begun. The schematics have been reviewed to guarantee the coherency of the signals exchanged between individual components and parts.

Also, a detailed examination of the code written thus/far has been completed with particular emphasis placed on the modifications necessary to accomodate the differences between the "software development system" (PDP8/e) and the microprocessor. The most salient differences concern the DMA and IOT instructions.

Presently the code is being modified to make certain that it will be microprocessor compatible and to achieve the highest degree of emulation possible before actual execution and testing is conducted on the microprocessor system.

Jeff Anderson

OTEMON (Project #95)

INTRODUCTION

A continuous waveform visual monitor is being designed in the form of a small, cheap TV controller. It is primarily intended for the display of natural phenomena such as EKG signals, although other applications can be envisioned.

The controller divides the TV screen into a number of "bands" along which the signal is displayed. The number of bands is variable, and the resolution changes accordingly.

PROJECT STATUS

The status of this project is essentially unchanged from last quarter. Construction of the prototype is awaiting receipt of parts.

Carlos Mier

4. Progress Report on New Projects Begun this Quarter

This section introduces new projects begun during this quarter.

4.1 ONR Funded Projects

SEQUENCY PROCESSING: BURST VERSION (Project #93)

<u>INTRODUCTION</u>

The basic problems of STOCHASTIC Processing (long integration time and correlation precautions) were resolved with great success by BURST PROCESSING, requiring only a minor increase in circuit complexity. However, one other problem afflicting BURST (and STOCHASTICS) is the larger data bandwidth required as compared to 4-bit binary processing. Thus, to minimize the "waste of bandwidth", a version of BURST, called SEQUENCY PROCESSING, has been proposed.

SEQUENCY PROCESSING uses a variable burst frame (as opposed to a fixed 10-slot frame in BURST), where the numerical information is carried by the number of time slots between signal level transitions (1 to 0, and 0 to 1). This may be visualized as analogous to quantized frequency modulation (Fig. 4.1). Thus, the duty cycle is always 50%. One must realize, however, that each frame of SEQUENCY information extends from one level transition to the next, not across a period as in a sine or square wave.

Information may be encoded using a comparator and a Block Sum Register (BSR), and may be decoded with a Sequency Transition Register (STR). Operations may be performed on the data by other SEQUENCY devices (adders, multipliers, etc.)

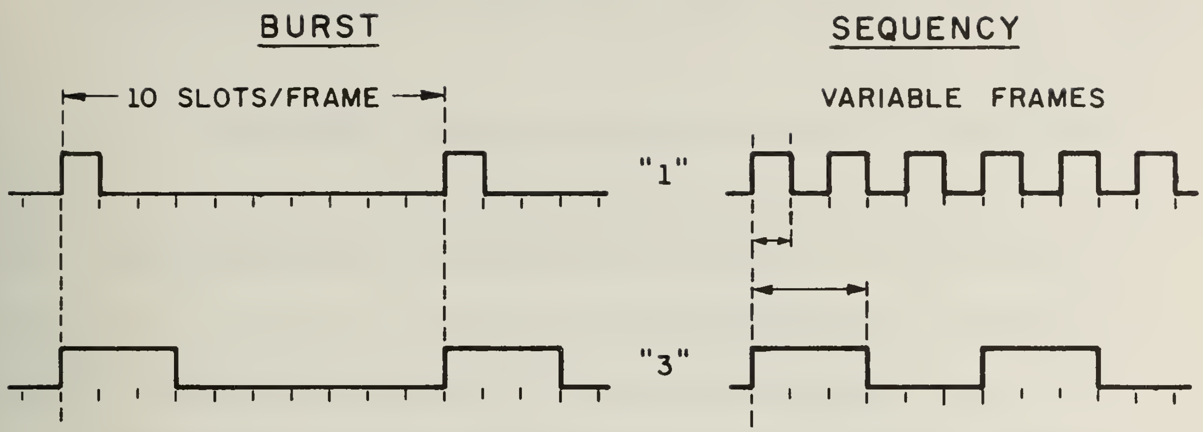

Figure 4.1 A comparison of BURST coding and SEQUENCY coding

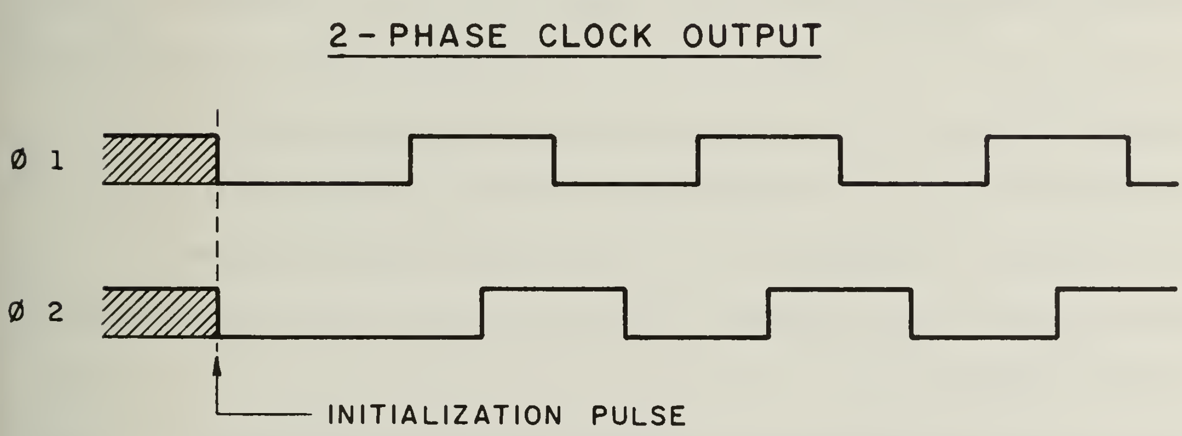

Figure 4.2 SEQUENCY Block Diagram

PROJECT STATUS

Initial design for the Sequency Encoder began in mid-August from preliminary proposal sketches. The analog signal may be encoded using the ramp encoder. That is:

1) The analog signal is fed into one side of a comparator.
2) A BSR output is fed into the other side.
3) A series of 1's are clocked into the BSR at a rate sufficient to satisfy the sampling theorem.
4) When the BSR output (proportional to the number of 1's) is greater than the signal, the comparator output toggles a flip-flop and clears the BSR to start the cycle over again.

This is just a ramp encoder with a flip flop on its output.

The actual circuit is slightly more complex than that described above in order to avoid a race condition in the toggling and clearing process. If the comparator output directly cleared the BSR, the clear pulse would be very narrow and of questionable integrity. To produce solid clearing pulses, a 2-phase clock was incorporated, where each phase is the same frequency, but one lags the other by 90 degrees, and is "self-orienting" so that the second phase never leads the first (Fig. 4.2). The circuit uses a 710 comparator, a 2.5 MHz clock and an 8-bit shift register for the BSR. The duration of the ramp is then 3.5 μs corresponding to a 286 kHz sampling rate.

The signal input frequency was increased to the point where any further increase introduced visible distortion into the encoding. This maximum frequency was 22.5 KHz. Thus, as determined empirically, the clock should be roughly 110 times the highest signal frequency.

Further work on this project has ceased because of lack of funding.

Ulrich B. Goerke

4.2 Non-ONR Funded Projects

Source of funds is given in brackets: [source]

MUMS II (#96) UNIVERSAL COMPILERS FOR MICROPROCESSORS

INTRODUCTION

The MUMS system is a network of several different microprocessors. To program this system efficiently it is useful to have a common high level language available. To accomplish this a pilot project has been undertaken to implement the language C on the MOS technology 6502 and the Intel 8080 micorprocessors.

The language C is very well suited to this application in as much as it allows efficient utilization of machine features while not requiring much in the way of translation facilities.

The compilers consist of three programs. The first program is the front end processor of an existing C compiler. Very few changes were required to use this program. It produces a file in an intermediate language [IL] which consists of assembler directives and a polish representation of expressions.

The second program serves as a linkage editor and can combine several IL files into one. Certain common machine independent transformations also are performed here. This serves to make the third program somewhat simpler.

The third program is called a COMP. It converts the IL into a core image file. It can be considered to be a hybrid of an assembler with a coder. It performs all allocation of space and all code generation. It reads the IL file twice and performs code generation twice so that the assembler can be a simple two pass assembler. All machine dependencies are in this program and as a result a change in processor requires only a change in this program.

PROJECT STATUS

A model COMP was initially written to test the system and is also used to serve as an example for the 6502 and 8080 COMPs. In order to allow the use of the C lanague on another microprocessor it is only necessary to write a COMP for that microprocessor. It took about eight man months to write three COMPS, the linkage editor and two interpreters.

The COMP for the 6502 generates interpretive code as well as an interpreter for this code. This was deemed necessary since the instruction set of the 6502 causes inefficient use of storage when programmed directly. The interpretive code is about 10 times smaller than that of the directly executed code.

The COMP for the 8080 produces considerably better code than the COMP for the 6502. A greater number of registers, available address arithmetic and a word-wise stack contributed to this as well as more care in optimization.

To date C programs have run on interpreters for both processors. C code has run on 8080 hardware and it is hoped that it will run on 6502 hardware in the near future.

Lawrence Lopez
George Lehmann

5. References

For an explanation of BURST Processing see:

Poppelbaum, Wolfgang J., "Statistical Processors", Advances in Computers, Vol. 14, pp. 188-230.

For a summary of previous work please refer to the 1976-77 Annual Report issued by the Department of Computer Science and to previous 1977-78 quarterly reports.

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20. ABSTRACT (Continue on reverse side if necessary and identify by block number)

This report presents the abstracts for reports on recently completed research projects, summary statements on the status of current projects, and explanations of new projects at the Information Engineering Laboratory of the Department of Computer Science at the University of Illinois at Urbana-Champaign.

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